APPENDIX D

Investigating switcher phase noise on 622 Mbit/s ATM PLL device

Test Setup

This section goes through an application demonstration searching for phase noise jitter caused by asynchronous interference, such as power supply switcher noise, using WAVECREST's DTS-2070C. This jitter source can cause crystal references, and PLL's driven by these references, to jitter at the period of the interference.

In many cases, the phase noise measured at the oscillator output is related to the noise rejection specifications of the devices' power supply circuit.

The following figures and illustrations show the test setup as well as the jitter identified, measured and displayed by WAVECREST's DTS-2070C and *Virtual Instrument* interface software.

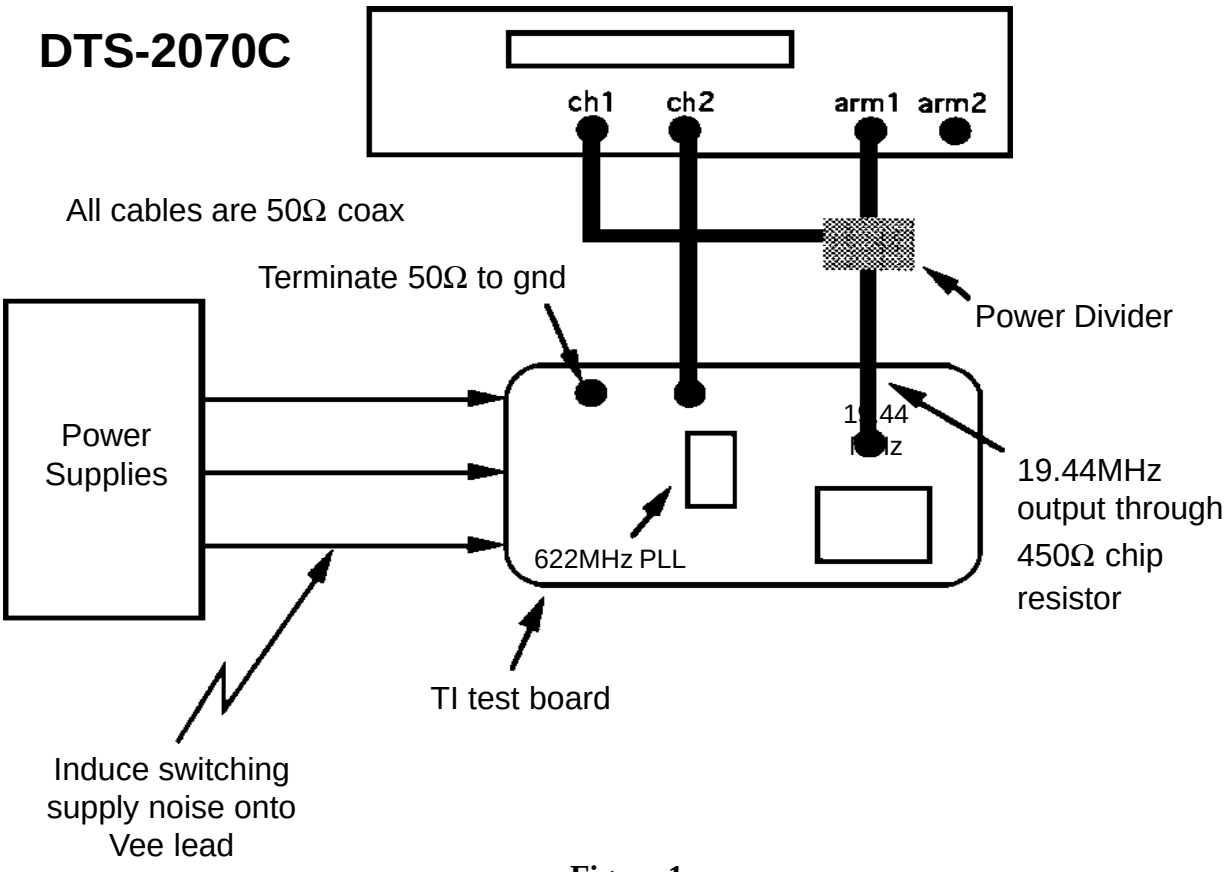

Figure 1

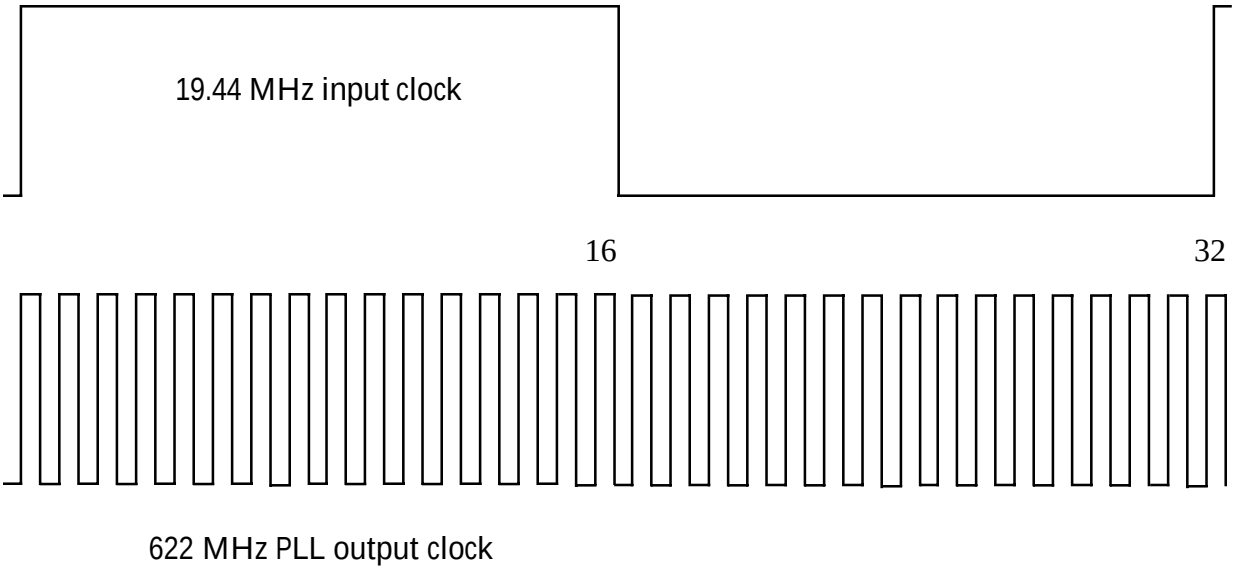

FIGURE 2

Figure 2 shows the count relationship of the 19.44 MHz input clock to the 622 MHz PLL output frequency. There are 32 outputs for every input cycle of the 19.44 MHz clock. In the following graphs the distortion of several of these cycles as a function of their placement with respect with in the input clock is illustrated.

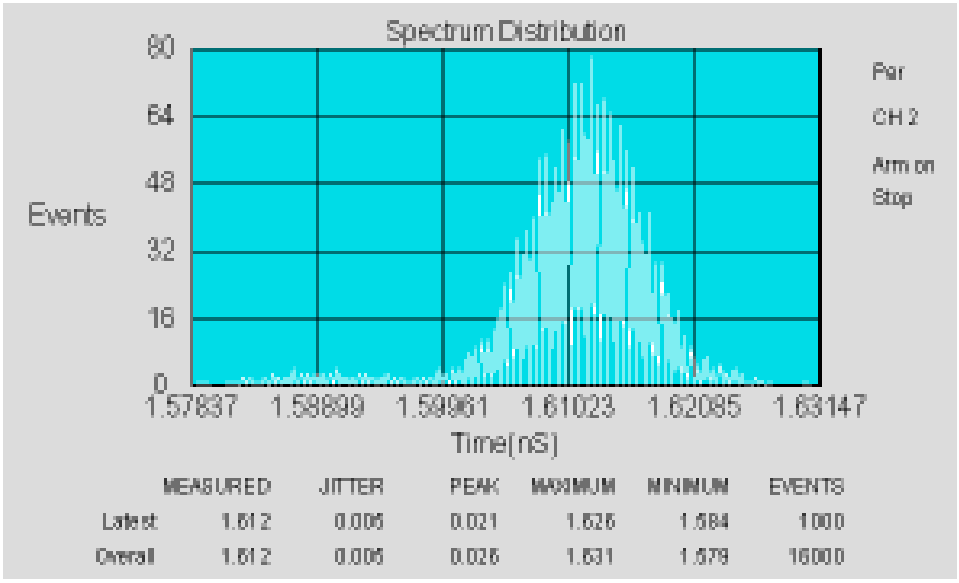

FIGURE 3

The first indication of a problem can be seen in Figure 3. The 622MHz output histogram shows offset short cycles down to 1.579ns.

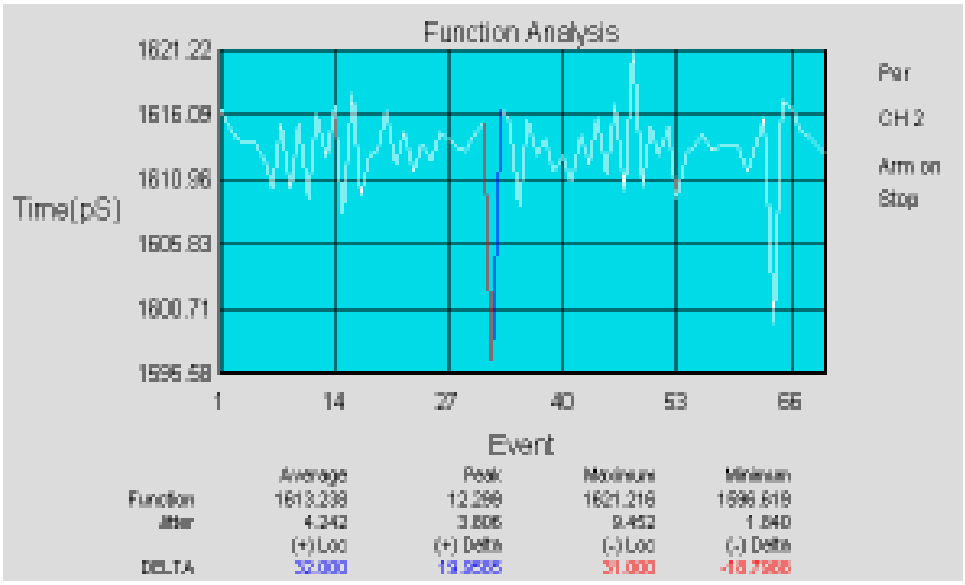

FIGURE 4

Looking at the same output pin of the device with the DTS' *VIRTUAL INSTRUMENT* Function Analysis window we can see that the output cycle directly adjacent to the falling edge of the input (the 32nd cycle) is short. The Function Analysis window is displaying the cycle-cycle output of
the DUT.

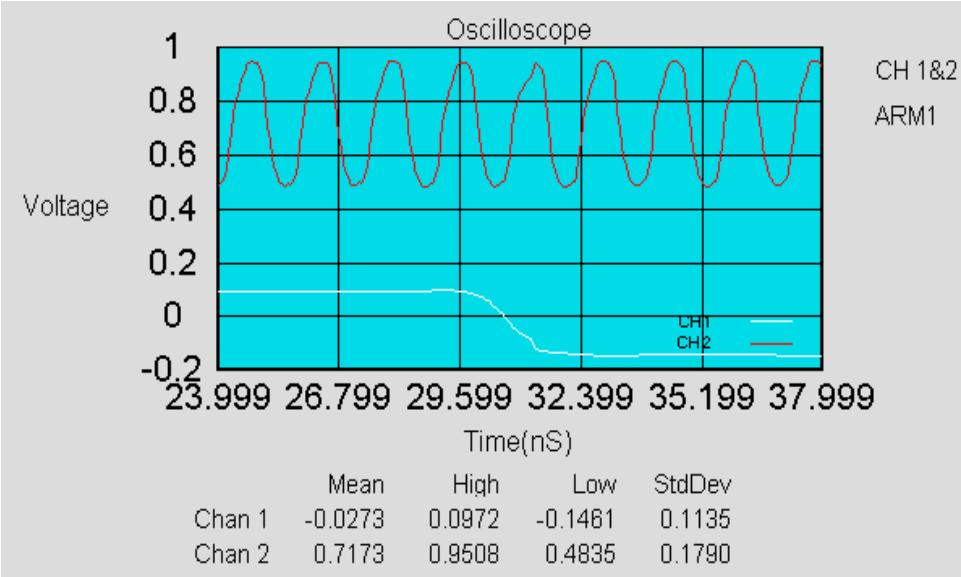

FIGURE 5

Using the Oscilloscope window on the DTS the user can digitize the waveforms on both channels. In figure 5, see the slight rise time distortion on channel 2 corresponding to the falling edge on channel 1. That slight distortion is causing the short cycle caught by the Function Analysis window.

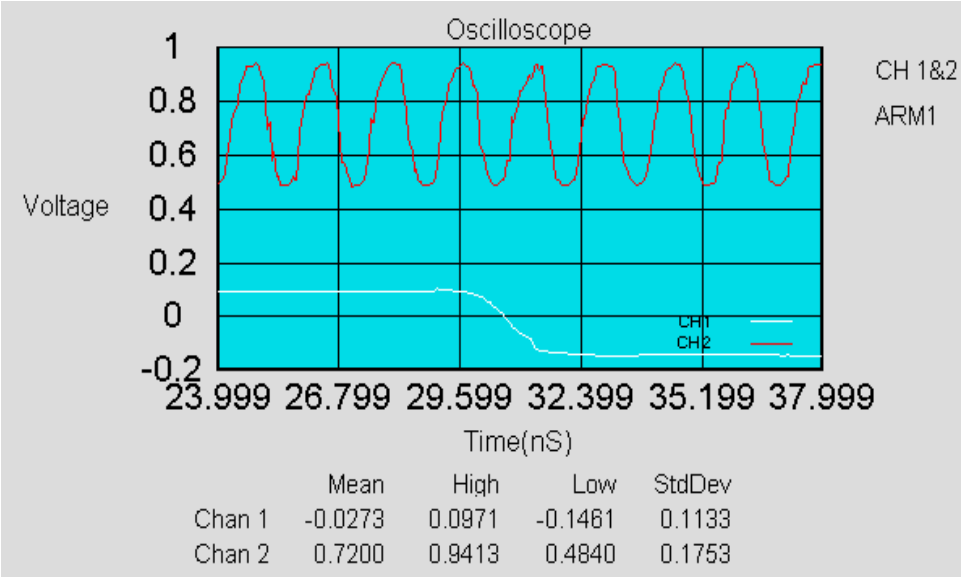

FIGURE 6

In Figure 6, the 130 kHz jitter on the input clock is showing up on channel 2 as a fuzzy trace when ever the VEE wire is placed near the switching power supply.

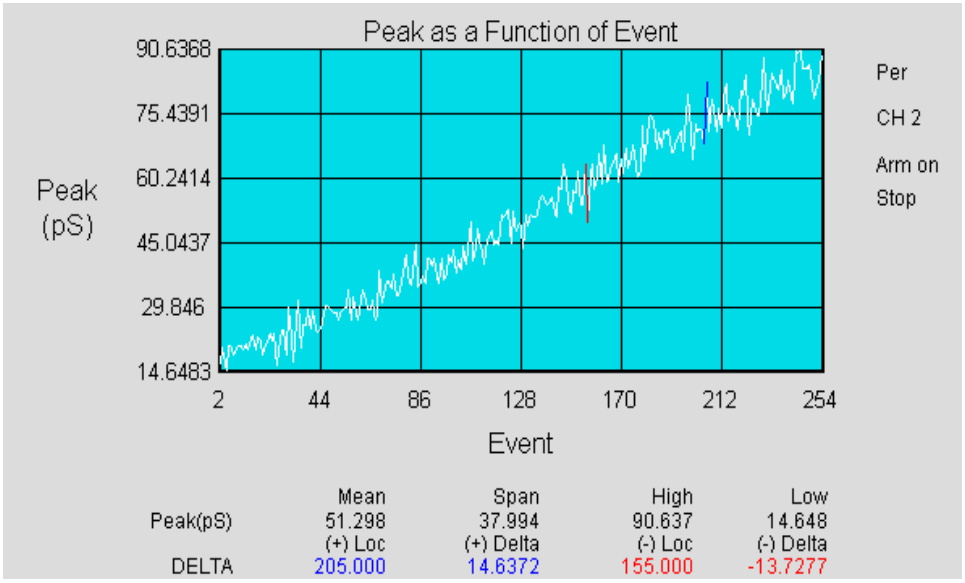

FIGURE 7

Further investigation of the output pin with the DTS' Jitter Analysis window showed that under some conditions the low frequency content of the phase noise of the 622 MHz output was higher than at other times. Compare figure 7 to Figure 8.

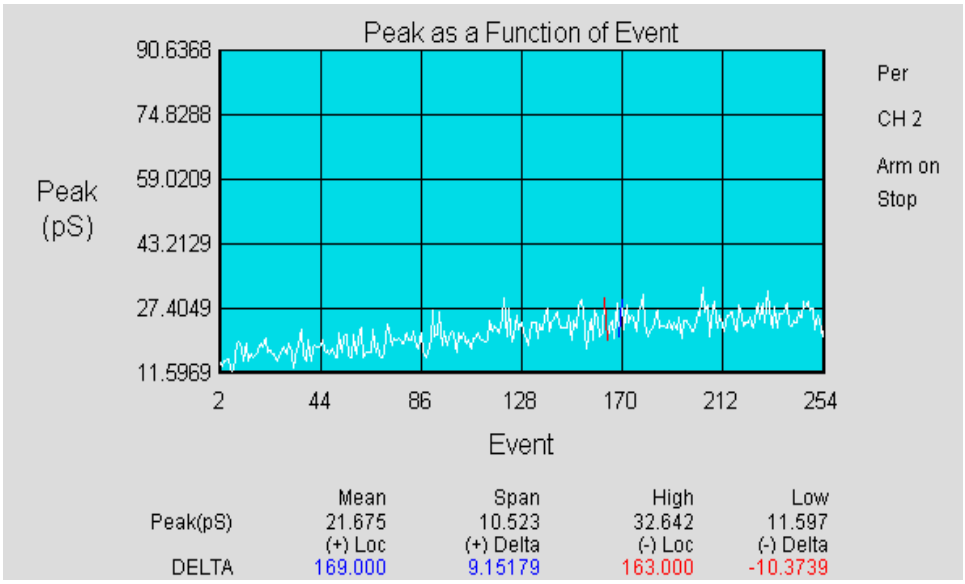

FIGURE 8

Figure 8 is showing much lower phase noise buildup than in Figure 7.

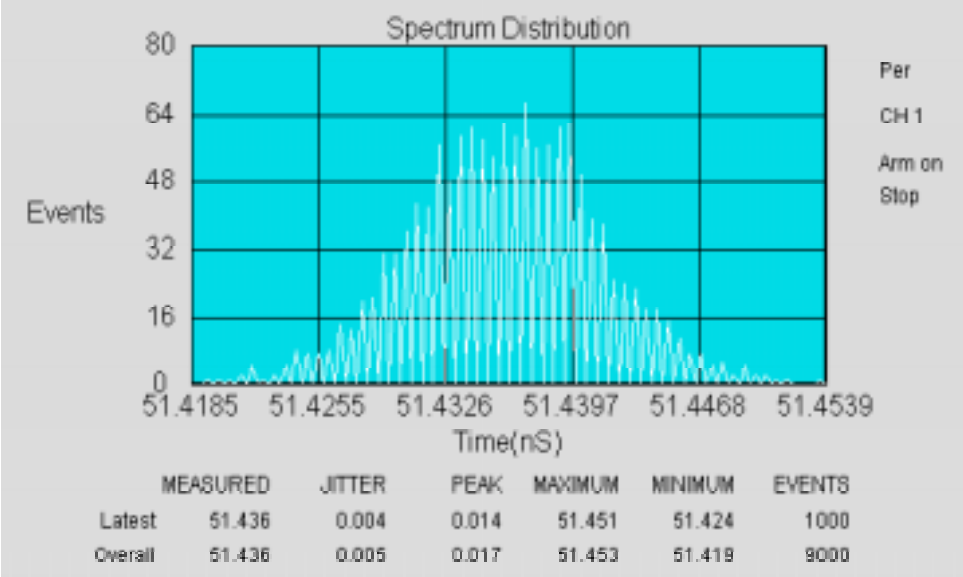

FIGURE 9

At first glance, Channel 1, which is the 19.44 MHz input, looks very nice with a low jitter rms value of 5ps.

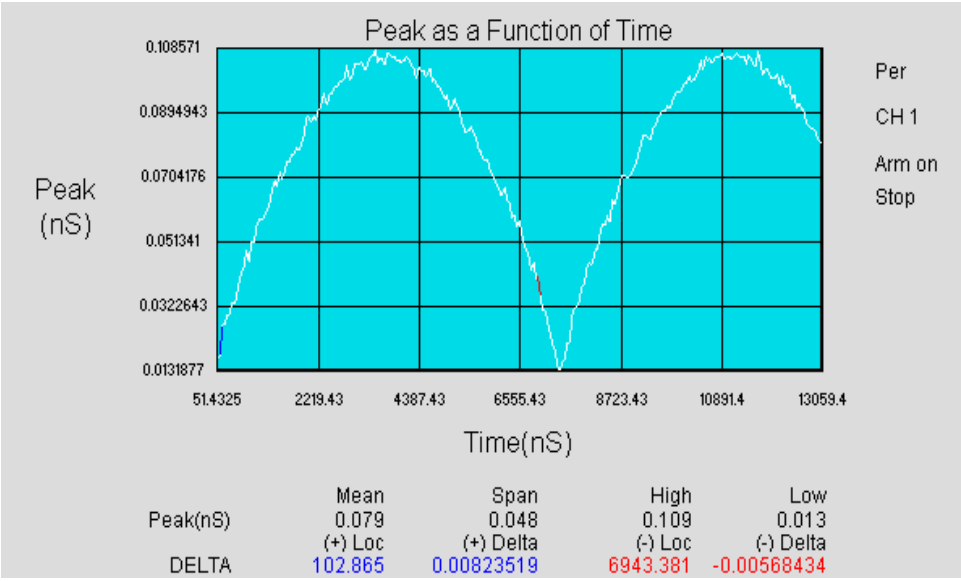

FIGURE 10

Using Jitter Analysis to look for low frequency phase noise showed an interfering signal riding on the input clock. The period of the interference was 7.7 microseconds. This corresponds to 130 kHz, which is the frequency of the switching power supply used to power this test demo.

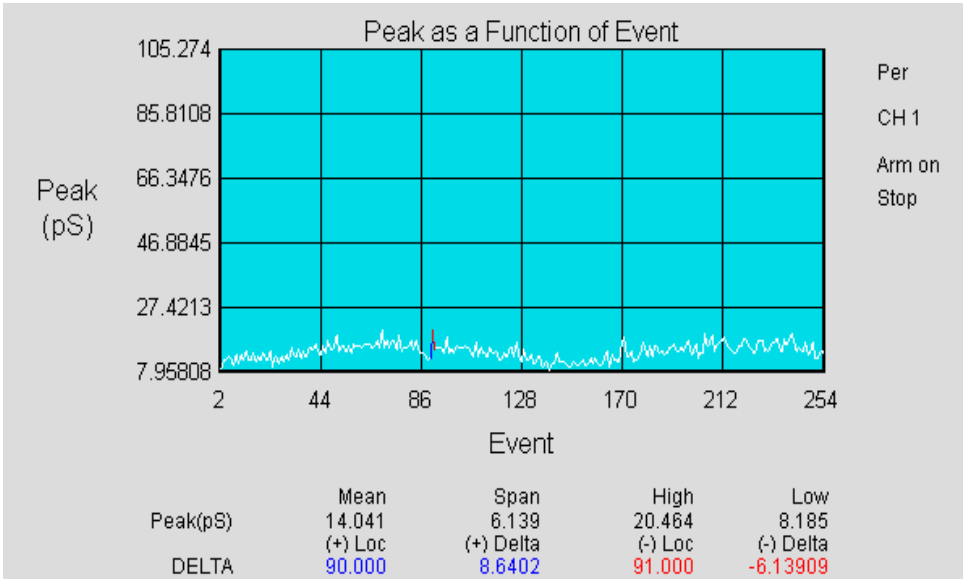

FIGURE 11

Whenever the VEE wire was placed near the power supply box, the jitter would increase. When the wire was moved away, the jitter would decrease. This corresponds to variations seen in Figures 5 and 6 as well. It would seem that the oscillator used to supply a reference to the PLL was causing the PLL to go out of specification.

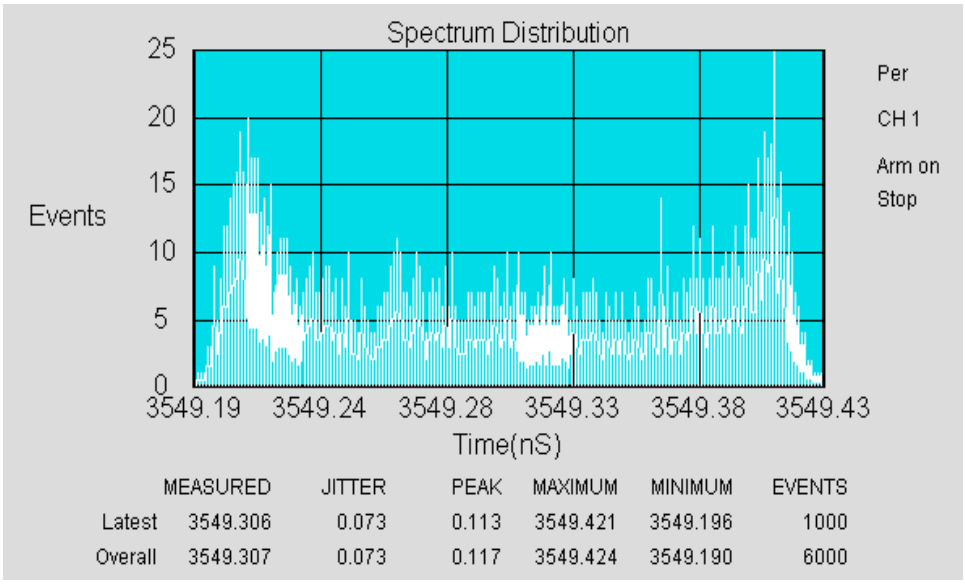

FIGURE 12

Using the Spectrum window the user can take a look at the histogram for the jitter on Channel 1 by setting the stop count on the DTS to where the peak jitter occurs, 70 cycles. Compare this with the display in Figure 9 which was looking for single-cycle jitter.

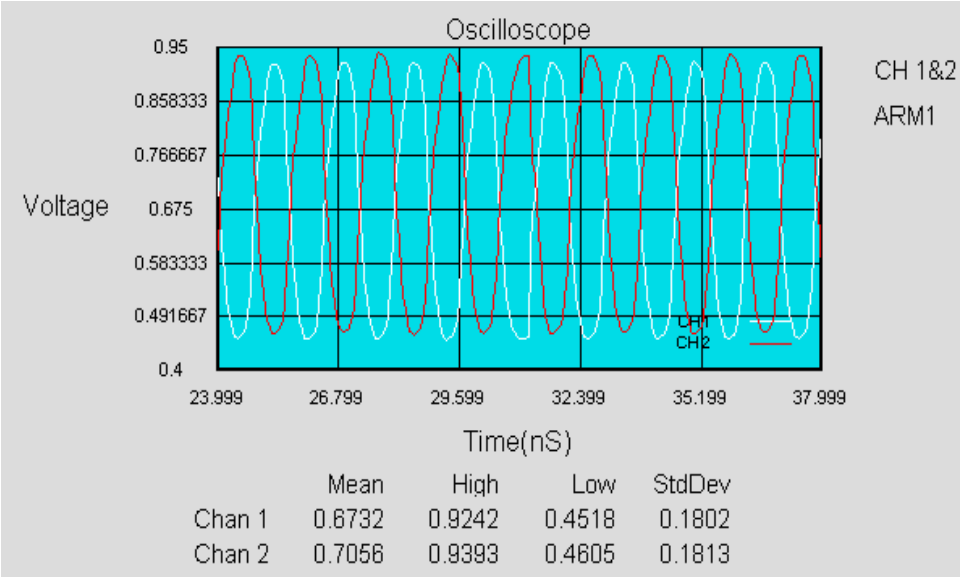

FIGURE 13

In Figure 13, the test setup was changed and Channel 1was connected to the complementary output of Channel 2 to look at the differential charateristics of the PLL.

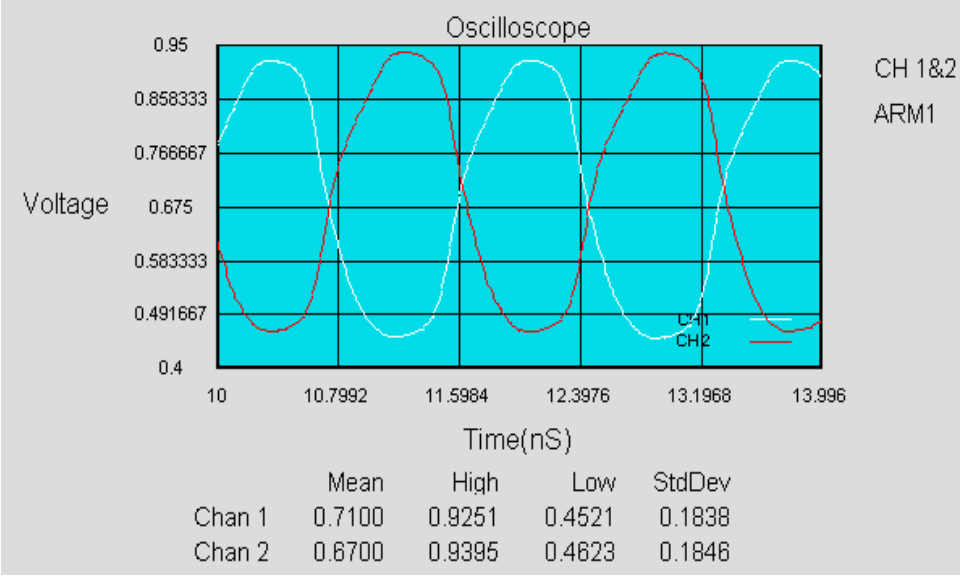

FIGURE 14

In Figure 14, the digitized window scaling has been adjusted for a closer view of the two signals.

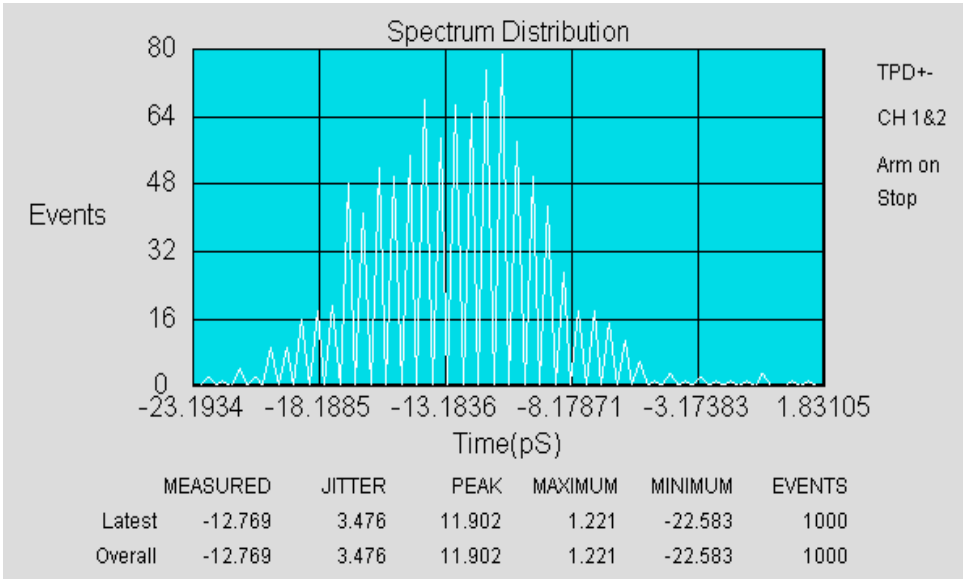

FIGURE 15

In Figure 15, the DTS is measuring the TPD+- at the complementary outputs. Notice the low jitter.

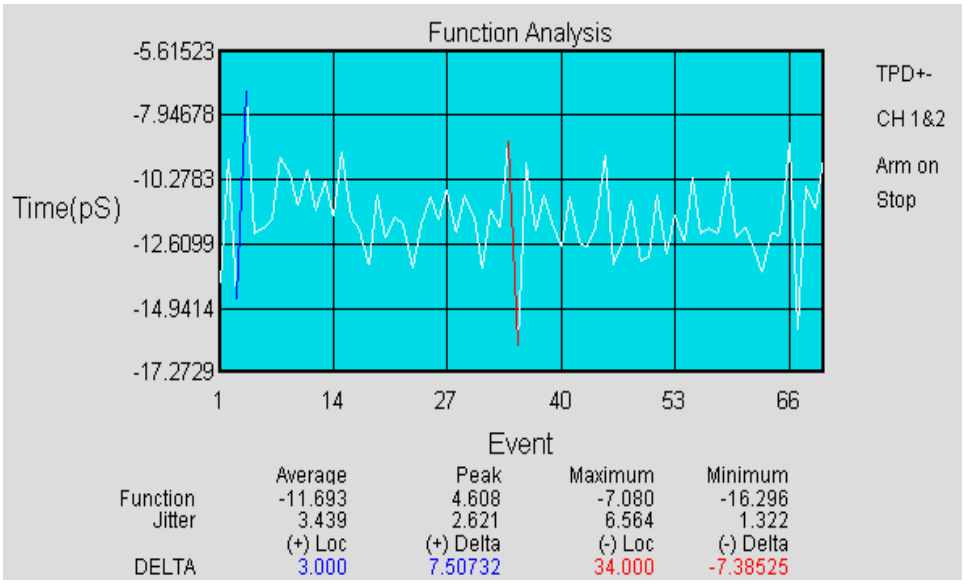

FIGURE 16

The Function Analysis window in *Virtual Instrument* enables the user to observe the 622MHz cycle-to-cycle crossing delay variations of each output and to detect anomalies.

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